IN THE CLAIMS

Please amend the claims to be in the form as follows:

Claim 1 (withdrawn)

Claim 2 (withdrawn)

Claim 3 (withdrawn)

Claim 4 (withdrawn)

Claim 5 (withdrawn)

Claim 6 (withdrawn)

Claim 7 (withdrawn)

Claim 8 (withdrawn)

Claim 9 (withdrawn)

Claim 10 (withdrawn)

Claim 11 (withdrawn)

Claim 12 (withdrawn)

Claim 13 (withdrawn)

Claim 14 (withdrawn)

Claim 15 (withdrawn)

Claim 16 (withdrawn)

Claim 17 (withdrawn)

Claim 18 (withdrawn)

Claim 19 (withdrawn)

Claim 20 (previously presented): A scalable MPEG2 compatible video decoder comprising:

at least one variable length decoder (304');

at least one inverse quantizer (310') coupled to said variable length decoder (300');

at least one inverse discrete cosine transform (312') coupled to said inverse quantizer (310');

at least one compensator (306) coupled to said variable length decoder (304');

a summing junction (314) coupled to said inverse discrete cosine transform (312') and motion compensator (306); and,

a controller (804);

wherein at least one of said variable length decoder (304'), inverse quantizer (310') inverse discrete cosine transform (312') and motion compensator (306) is coupled to said controller and responsive thereto to operate in one of a plurality of modes each having a given complexity characteristic for an acceptable distortion level of an output of said decoder; and, wherein said controller selects said one of said modes based upon said given complexity characteristics.

Claim 21 (previously presented): A scalable MPEG2 compatible video decoder according to Claim 20, wherein said controller selects said one of said modes further based upon an available amount of computing resources for operating at least one of said variable length decoder (304'),

inverse quantizer (310'), inverse discrete cosine transform (312') and motion compensator (306').

Claim 22 (previously presented): A scalable MPEG2 compatible video decoder according to Claim 20, wherein said at least one inverse discrete cosine transform (312') includes a plurality of inverse discrete cosine transforms (312, 312', 312") which is selectively operable in response to said controller (804).

Claim 23 (previously presented): A scalable MPEG2 compatible video decoder according to Claim 22, wherein said selectively operated inverse discrete cosine transform (312, 312', 312") implements said selected one of said modes.

Claim 24 (previously presented): A scalable MPEG2 compatible video decoder according to Claim 23, wherein said complexity-distortion characteristic of said selected one of said modes is more efficient than those of the others of said plurality of modes.

Claim 25 (withdrawn)

Claim 26 (withdrawn)

Claim 27 (new) A scalable MPEG2 compatible video decoder according to Claim 20, further comprising at least one scaleable application (300') that is responsive to said controller (804).

Claim 28 (new) A scalable MPEG2 compatible video decoder according to Claim 27, wherein said scaleable application (300') is operable in a plurality of modes, each of said modes having a different complexity characteristic.

Claim 30 (new) A scalable MPEG2 compatible video decoder according to Claim 28, wherein said controller (804) determines if available resource are not suitable for operation of said scaleable application (300') and selects another of said modes for said scaleable application (300').

Claim 31 (new) A scalable MPEG2 compatible video decoder according to Claim 20, further comprising a memory accessible to said controller (804).

Claim 32 (new) A scalable MPEG2 compatible video decoder according to Claim 32, wherein said memory includes data indicative of complexity-distortion characteristics of each of said modes for a plurality of amount of available system resources.

Claim 33 (new): A method for a scalable MPEG2 compatible video decoder comprising the steps of:

providing said scalable MPEG2 compatible video decoder with at least one variable length decoder (304') coupled to at least one inverse quantizer (310'), with at least one inverse discrete cosine transform (312') coupled to said inverse quantizer (310'), at least one compensator (306) coupled to said variable length decoder (304'), a summing junction (314) coupled to said inverse discrete cosine transform (312') and said motion compensator (306); and a controller (804);

coupling said variable length decoder (304'), inverse quantizer (310') inverse discrete cosine transform (312') and motion compensator (306) is coupled to said controller; and

responding with at least one of said variable length decoder (304'), inverse quantizer (310') inverse discrete cosine transform (312') and motion compensator (306) is coupled to said controller to operate in one of a plurality of modes each having a given complexity characteristic for an acceptable distortion level of an output of said decoder; and, wherein said controller selects said one of said modes based upon said given complexity characteristics.

Claim 34 (new): A method for a scalable MPEG2 compatible video decoder according to Claim 33, further comprising the step of said controller selecting one of said modes further based upon an available amount of computing resources for operating at least one of said variable length decoder (304'), inverse quantizer (310'), inverse discrete cosine transform (312') and

motion compensator (306').

Claim 35 (new): A method for a scalable MPEG2 compatible video decoder according to Claim 33, wherein the step of providing further comprises said at least one inverse discrete cosine transform (312') including a plurality of inverse discrete cosine transforms (312, 312', 312") which is selectively operable in response to said controller (804).

Claim 36 (previously presented): A method for a scalable MPEG2 compatible video decoder according to Claim 35, wherein said selectively operated inverse discrete cosine transform (312, 312', 312") implements said selected one of said modes.

Claim 37 (new): A method for a scalable MPEG2 compatible video decoder according to Claim 36, wherein said complexity-distortion characteristic of said selected one of said modes is more efficient than those of the others of said plurality of modes.

Claim 38 (new): A method for a scalable MPEG2 compatible video decoder according to Claim 33, wherein the step of responding further comprises at least one scaleable application (300') responding to said controller (804).

Claim 39 (new): A method for a scalable MPEG2 compatible video decoder according to Claim 38, wherein said scaleable application (300') is operable in a plurality of modes, each of said modes having a different complexity characteristic.

Claim 40 (new): A method for a scalable MPEG2 compatible video decoder according to Claim 39, further comprises the step of selecting another of said modes for said scaleable application (300') if available resource are not suitable for operation of said scaleable application (300').

Claim 41 (new) A method for a scalable MPEG2 compatible video decoder according to Claim 33, wherein the step of providing further comprises a memory accessible to said controller (804) that includes data indicative of complexity-distortion characteristics of each of said modes for a plurality of amount of available system resources.